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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,262	11/17/2003	Erick M. Hirata	03T005	4589

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EXAMINER	
NGUYEN, LINH V	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,262	HIRATA ET AL.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *39 and 40* is/are allowed.

6)☒ Claim(s) *1-8,18-25,29-35,41 and 42* is/are rejected.

7)☒ Claim(s) *9-17,26-28 and 36-38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/715,262 filed on 11/17/2003. Claims 1 – 42 are pending on this application.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

3. In claim 26, there is no antecedent basis for the wording, "said node A " of resistive network. There is not reference to "node" in earlier the dependent claims 25, 2 and 1, either in the form of an implied as well as a literal description from which an earlier antecedent reference may be made. Although, the disclosure does make reference to nodes of resistive network, there is no clear recitation in these claims to avoid possible confusion as to what is actually claimed. The claims fail to particularly point out and distinctly claim the subject matter that the applicant considers to be the invention here. Clarification is required.

According, claims 27 – 28 are object because depended upon the object claim 26.

Claims 25 - 28 not been further treat on merits on this office action.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 – 8, 22 – 25, 29, and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Iizuka U.S. patent No. 5,585,751.

Regarding claim 1, Fig. 3 discloses a current source comprising (19): first means (31) for generating a current (delta I2) in response to an applied voltage (output of 21) and a resistance variable (9 – 13) in response to a control signal (Col. 3 lines 35 – 37), and second means (8) for supplying said control signal.

Regarding claim 2, wherein said first means includes a resistive network comprising a first plurality of resistors R.sub.a, R.sub.b, . . . , R.sub.m (10– 13).

Regarding claim 3, wherein said first plurality of resistors R.sub.a, R.sub.b, R.sub.m (10 – 13) are connected in parallel across a first node A (top node of 10 – 13) and a second node B (bottom node of 14 – 18).

Regarding claim 4, wherein said resistive network further includes a first plurality of switches S.sub.1, S.sub.2, . . . S.sub.m (14 – 18) each switch coupled to one of said first plurality of resistors R.sub.a, R.sub.b, . . . , R.sub.m (10 – 13) and adapted to

switch said resistor in and out of said resistive network in response to said control signal (Col. 3 lines 35 – 37).

Regarding to claim 5, wherein said control signal is a digital word comprised of m bits (Col. 5 lines 30 – 32).

Regarding claim 6, wherein each bit of said control signal controls one of said switches S.sub.1, S.sub.2, . . . S.sub.m (Col. 5 lines 30 – 32).

Regarding claim 7, wherein said first plurality of resistors R.sub.a, R.sub.b, . . ., R.sub.m are binary weighted (KR – 4KR).

Regarding claim 8, wherein said resistive network further includes a resistor R2 (9) connected between node A and node B.

Regarding claim 22, wherein said first means further includes a transistor Q (31) adapted to apply a voltage across said resistive network (9 – 13) to generate a current I (delta I2).

Regarding claim 23, wherein a reference voltage V.sub.REF (output of 21) is applied to the base of said transistor Q (31).

Regarding claim 24, wherein said current I (delta I2) is output from the collector of said transistor Q (31).

Regarding claim 25, wherein a first end of a resistor R1 is coupled (32) to the emitter of said transistor Q (31).

Regarding claim 29, Fig. 1 of Iizuka disclose current source (19) comprising: a transistor Q (31) adapted to receive a voltage V.sub.REF (output of 21) at its base and output a current I at its collector (delta I2); a resistive network (9 – 13) coupled to the

emitter of said transistor Q (31), said resistive network including a plurality of resistors R.sub.a, R.sub.b, . . . , R.sub.m (9 – 13); a circuit (8) for supplying a digital control signal (Col. 3 lines 35 – 37); and a plurality of switches S.sub.1, S.sub.2, . . . S.sub.m (14 – 18) each switch coupled to one of said plurality of resistors R.sub.a, R.sub.b, . . . , R.sub.m (9 – 13) and adapted to selectively switch said resistor in and out of said resistive network in response to said control signal (Col. 3 lines 35 – 37).

Regarding claim 41, Fig. 3 of Iizuka et al. discloses a method for trimming a current source (delta I) including the steps of: creating a resistive network comprised of a plurality of resistors (9 – 123); applying a voltage across said resistive network to generate a current I (delta I2); and selectively switching (14 – 18) said resistors in and out of said resistive network (9 – 13) until said current I is at a desired value (delta I).

6. Claims 31, 32, 33 and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Kiriaki U.S. patent No. 6,337,648.

Regarding claim 31, Fig. 1 of Kiriaki discloses a current source (14) comprising: two resistors R1 and R3 connected in series (6, 7, 8); first means (10 - 12) for applying a voltage across said resistors R1 and R3 (6 – 8) to generate a current I (current flows through 6 – 8); a digital to analog converter (A, B) adapted to apply a voltage (voltage at 6 and 8 when current flow through) or current at the node between said resistors R1 and R3 (nodes between 6 – 8) to change the current I in response to a control signal input to said DAC (9 – 10); and second means for supplying said control signal (Switch binary states set by Digital input Vdig).

Regarding claim 32, wherein said DAC is a voltage output DAC adapted to change the voltage at said node between R1 and R3 (this is inherent to fig. 3, because if the voltage at 2 – 5 change then the voltage at the nodes between 6 – 7 will changes.

Regarding claim 33, wherein said DAC is a current output DAC adapted to add a current at said node between R1 and R3 (this is inherent to fig. 3, because the current is adding to the nodes between 6 – 8 by the voltage at 2 – 5).

Regarding claim 42, Fig. 1 of Kiriaki discloses a method for trimming a current source (14) including the steps of: connecting two resistors R1 and R3 in series (6, 7); applying a first voltage across said resistors R1 and R3 to generate a current I (Current flows through 6 and 7); and connecting the output of a digital to analog converter (I_{DAC-}, I_{DAC+}) to the node between R1 and R3 (node between 6 and 7); changing the digital input (Switch binary states set by digital input V_{Dig}) to said digital to analog converter (Fig. 1) until said current I (current flow through 6, 7, 8) is at a desired value.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 18 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iizuka as applied to claim 4 above, in further view of Bae U.S. Patent No. 6,831,580.

Regarding claims 18 and 19, Iizuka as applied to claim 4 above, fails to disclose the switches (14 – 18) are implemented using NMOS transistors.

Fig. 5 of Bae discloses a resistor network (100) having switches (B1 – B3) are implemented using NMOS transistors.

Iizuka and Bae are common subject matter for switching of resistive network. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the switching of Iizuka by using NMOS transistors, as has taught by Bae, since switches implemented by NMOS transistor is well known and conventional to one ordinary skill in the art. Furthermore, implement the switches by MOS technology is providing miniaturizing products as well as reducing production cost (Bae, Col. 1, lines 35 – 36).

Regarding claim 20, Iizuka in combined with Bae as applied to claim 19 above, further discloses wherein the number of transistors (B1 – B3) used to implement each switch is determined by the weight of the resistor (Iizuka, Fig. 3 [0KR-4KR]) that the switch is coupled to.

Regarding claim 21, Iizuka in combined with Bae as applied to claim 18 above, further disclosed wherein said switches are controlled by control signals (b1 – b3) applied to the gates of said transistors.

9. Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiriaki as applied to claim 31 above, in further view of Iizuka as applied to claim 1 above,

Regarding claims 34 and 35, Kiriaki as applied to claim 31 above, fails to disclose the first mean (14 – 18) includes a transistors and a reference voltage V.sub.REF is applied to the base of said transistor Q.

Fig. 3 of Iizuka as applied to claim 1 above, disclose first mean (31) includes a transistors (Q) and a reference voltage (output of 21) is applied to the base of said transistor Q.

Kiriaki and Iizuka a common subject matte for current generator in digital to analog converter. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated the transistor taught by current generator of Iizuka into Kiriaki for the purpose to providing a selected current from controlling transistor.

10. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA (Applicant Admitted Prior Art), in view of Iizuka U.S. Patent No. 5,585,751.

Fig. 2 of AAPA disclose digital to analog converter comprising: a first current summing bus (16); a second current summing bus (18); and a plurality of current steering cells (12'), each cell including: a current source (20, 24) comprising: a transistor Q (Fig. 4 [Q]) adapted to receive a voltage V.sub.REF (Fig. 4 [VREF]) at its base and output a current (Fig. 4 [I]) at its collector; a resistive network (Fig. 4 [R1, Rvar]) coupled to the emitter of said transistor (Fig. 4 [Q]), said resistive network including a first plurality of resistors (Fig. 4 [R1, Rvar]) and a pair of transistors (Q1, Q2) for selectively switching current (I1, I2) from said current source (Ibit1) between said first current

summing bus (16) and said second current summing bus (18) in response to an input signal (Vs1, Bar VS1). However, AAPA fails to disclose a circuit for supplying a digital control signal; and a first plurality of switches S.sub.1, S.sub.2, . . . S.sub.m, each switch coupled to one of said first plurality of resistors R.sub.a, R.sub.b, . . . , R.sub.m and adapted to selectively switch said resistor in and out of said resistive network in response to said control signal.

Fig. 3 of Iizuka discloses a digital to analog converter (8) having a circuit for supplying a digital control signal (Col. 3 lines 35 – 37); and a first plurality of switches S.sub.1, S.sub.2, . . . S.sub.m (14 – 18) each switch coupled to one of said first plurality of resistors R.sub.a, R.sub.b, . . . , R.sub.m (9 – 13) and adapted to selectively switch said resistor in and out of said resistive network in response to said control signal (Col. 3 lines 35 – 37);

AAPA and Iizuka are common subject matter for digital to analog converter. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the switching resistive network taught by Iizuka into AAPA for the purpose of providing a current generator depending upon selected value of resistive network from digital frequency control signal (Iizuka, Col. 2 lines 14 – 19).

Allowable Subject Matter

11. Claims 9 – 17 and 36 - 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 39 and 40 are allowed.

Cited References

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited of reference is relating to reference buffer.

Contact Information

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

3/10/05

Linh Van Nguyen 

Art Unit 2819